IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re DIVISIONAL PATENT APPLICATION OF

MATSUDA et al.

Group Art Unit: 2818

Appln. No.: UNASSIGNED

Examiner: Dung Anh LE

Filed: HEREWITH

Atty Dkt 008312/0304355
C# M#

Title: SEMICONDUCTOR DEVICE COMPRISING BURIED CHANNEL REGION AND METHOD FOR MANUFACTURING THE SAME

June 24, 2003

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INFORMATION DISCLOSURE STATEMENT

Attached is Form PTO-1449 listing all of the documents cited by Applicant and the PTO in the parent application(s) relied upon under 35 USC 120. Per Rule 98(d) copies of those documents are not enclosed.

Please consider those documents and advise that they have been considered in this new application by returning a copy of the enclosed Form PTO-1449 with the Examiner's initials in the left column per MPEP 609. .

Respectfully submitted,

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FORM PTO-1449 (modified)
To: U.S. Department of Commerce
(PW FORM PAT-1449)
Patent and Trademark Office

Atty. Dkt. No.	M#	Client Ref.
	0304355	T1KK-01S1349-D

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

Applicant: MATSUDA et al.

Appln. No.: UNASSIGNED

Filing Date: June 24, 2003

Date: June 24, 2003 Page 1 of 1

Examiner: D. LE | Group Art Unit: 2818

U.S. PATENT DOCUMENTS

Examiner's Initials*		Document Number	Date MM/YYYY	Name (Family Name of First Inventor)	Class	Sub Class	Filing Date (if appropriate)
	AR	6,319,807	11/2001	Yeh et al.			
	BR	6,353,249	03/2002	Boyd et al.			
	CR	5,856,225	01/1999	Lee et al.			
	DR	6,087,208	07/2000	Krivokapic et al.			
	ER						
	FR						
	GR						
	HR						
	IR						
	JR						
	KR						
	LR						
	MR						
	NR						

FOREIGN PATENT DOCUMENTS

		Document Number	Date MM/YYYY	Country	Inventor Name		English Abstract		Translation Readily Available	
							Enclosed	No	Enclose	No
	OR									
	PR									
	QR									
	RR									
	SR									
	TR									
	UR									

OTHER (Including in this order Author, Title, Periodical Name, Date, Pertinent Pages, etc.)

	VR	A. Chatterjee et al., "Sub-100nm Gate Length Metal Gate NMOS Transistors Fabricated by a Replacement Gate Process," IEDM, 1997, pp. 821-824
	WR	A. Chatterjee et al., "CMOS Metal Replacement Gate Transistors Using Tantalum Pentoxide Gate Insulator," IEDM, 1998, pp. 777-780
	XR	Yagishita et al., "High Performance Metal Gate MOSFETs Fabricated by CMP for 0.1um Regime," IEDM 1998, pp. 785-788
	YR	
	ZR	
	AAR	

Examiner | Date Considered:

*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP § 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to Applicant.